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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,535	09/24/2004	Ko-Hsing Chang	11041-US-PA-1	5534

31561 7590 08/23/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
SCHILLINGER, LAURA M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

10

Office Action Summary	Application No.	Applicant(s)	
	10/711,535	CHANG ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee ('525).

Lee teaches the following claimed limitations as cited below:

1 . A method of fabricating a flash memory cell, comprising the following steps:

providing a substrate (Fig.2A(1));

forming a first opening (3) and a second opening (5) in the substrate, wherein the second opening (5) is formed on the bottom of the first opening (3), the second opening is narrower but is deeper (5), as measured from the surface of the substrate, than the first opening (3) (Fig.2A and 2B);

forming a high-voltage doped region under the bottom of the second opening in the substrate (Fig.2C and Fig.2F);

forming a gate dielectric layer on the substrate in the first opening and the second opening (Fig.2G (8));

forming a first conductive spacer on a sidewall of the first opening as a select gate, and forming a second conductive spacer on a sidewall of the second opening as a floating gate (Fig.2L (9a and 9b), see also Fig. 2M (12a)); and

forming a source region beside the first opening in the substrate (Fig.2F).

2. The method of fabricating a flash memory cell of claim 1 , wherein the step of forming the first opening comprises: forming a mask layer (PR) with the pattern of the first opening over the substrate and etching the substrate with the mask layer as mask to form the first opening (Fig.2A).

3. The method of fabricating a flash memory cell of claim 2, wherein the first opening has round corners on its bottom (Fig.2G- the oxide rounds the corners).

4. The method of fabricating a flash memory cell of claim 2, wherein the step of forming the second opening comprises: forming spacers on the sidewalls of the mask layer and the first opening', and etching the substrate, with the mask layer and the spacers as mask, to form the second opening (Fig.2B).

5. The method of fabricating a flash memory cell of claim 4, wherein the second opening has round corners on its bottom (Fig.2G- the oxide rounds the corners).

6. The method of fabricating a flash memory cell of claim 4, wherein the process to form the high-voltage doped region under the bottom of the second opening in the substrate comprises a step of ion implantation, with the mask layer and the spacer as mask, to the substrate (Fig.2F) .

8. The method of fabricating a flash memory cell of claim 1 , wherein the process to simultaneously form the first and the second conductive spacers comprises: forming a conformal conductive layer on the substrate', and anisotropic etching the conformal conductive layer to form the first conductive spacer on the sidewalls of the first opening and the second opening (Fig.2I-2J))).

9. The method of fabricating a flash memory cell of claim 8, wherein the materials of the conformal conductive layer comprise polysilicon (Col.3, lines: 35-50).

10. The method of fabricating a flash claim 1 , the method further comprises: memory cell of forming an insulating layer on the substrate, where the insulating layer covers the select gate and the floating gate; and forming a contact plug which penetrates through the insulating layer and is electrically connected with the high-voltage doped region (Fig.2O (14)).

11 . The method of fabricating a flash memory cell of claim 1 0, the method further comprises a step, before the formation of the insulating layer, to form an insulating spacer on another sidewalls of the select gate and the floating gate so as to protect the floating gate in the process of forming the contact plug (Fig.2O (11 and 13)).\

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee ('525).

In reference to claim 7, Lee teaches the method of fabricating a flash memory cell of claim 1, however fails to explicitly teach wherein the process to form the gate dielectric layer on the surface of the substrate in the first opening and the second opening comprises thermal oxidation. Lee is not specific as to the method of forming the oxide layer; however thermal oxidation is a well known technique for forming gate oxides in the field of semiconductor manufacturing and such a limitation would have been obvious to one of ordinary skill in the art at the time the invention was made.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Laura M Schillinger
Primary Examiner
Art Unit 2813

08/16/06